Claims 23-28

Claims 23-28 are objected to as being dependent upon a rejected base claim, but would be allowable if re-written in independent form to include the limitations of the rejected base claim and any intervening claims.

In response thereto, Claim 23 is re-written in independent form to include the limitations of base Claim 21 and intervening Claim 22, and is therefore now patentable.

Claims 24-28 depend from Claim 23 and therefore distinguish over the cited references for the same reasons as Claim 23.

Claim Rejections

Rejection of Claims under 35 USC §102 over Feldmeier '886

Claims 29-32, 36, and 73-74 are rejected under 35 USC §102(b) as anticipated by U.S. Patent No. 5,920,886 to Feldmeier (hereinafter referred to as Feldmeier '886). Applicants respectfully traverse these rejections, as discussed below.

Claims 29-32 and 36

Applicants' Claim 29 (as amended) recites:

A content addressable memory (CAM) system, comprising:

an array of binary CAM cells segmented into a plurality of array groups, each array group assigned a priority and each array group including a plurality of rows of CAM cells;

a plurality of group global masks, each for storing a mask pattern indicating priority of a corresponding array group; and

a priority table including a plurality of rows, each for storing the priority of a corresponding array group.

Feldmeier '886 neither discloses nor suggests the CAM system recited in Applicants' Claim 29.

Feldmeier '886 discloses a system for storing ternary hierarchical address values "in a binary CAM by breaking the ternary address into two components: a binary address and a priority mask" (col. 7, lines 31-37). "The binary address values are stored in the CAM, while the mask values are stored in a separate mask list" (col. 7, lines 38-40). As illustrated in Feldmeier '886's FIG. 10B, each binary address value is stored in a row of binary CAM 1020, and each associated priority mask is stored in a corresponding row of priority CAM 1040. Thus, each priority mask stored in Feldmeier '886's priority CAM 1040 indicates a priority for only one data word stored in its binary CAM 1020.

This is in contrast to the CAM system of Applicants' Claim 29, where each group global mask indicates priority of a corresponding array group that includes a plurality of rows of CAM cells. Thus, each mask value stored in a group global mask of the system of Applicants' Claim 29 may indicate priority for a plurality of data values (e.g., binary address values) stored in the plurality of rows of an associated array group.

The Examiner seems to equate a row of Feldmeier '886's CAM array 1020 with one of the array groups recited in Applicants' Claim 29. However, while each array group recited in Applicants' Claim 29 includes a plurality of rows of CAM cells for storing a plurality of data values whose priority is indicated by a single corresponding mask value, each mask value stored in Feldmeier '886's priority CAM 1040 indicates priority for only one data value stored in a single corresponding row of binary CAM 1020. Indeed, there is no language in Feldmeier '886 that discloses or suggests a CAM system that includes a plurality of array groups each having a plurality of rows of CAM cells and that includes a plurality of group global masks each for indicating priority of

a corresponding plurality of rows of CAM cells, nor has the Examiner pointed to any such language.

To anticipate a claim under 35 USC §102, each and every element of the claim must be disclosed in a single reference (*Corning Glass Works v. Sumitomo Electric*, 9 USPQ2d 1962, 1965 (Fed. Cir. 1989)). The exclusion of a claimed element, no matter how insubstantial or obvious, from a prior art reference is enough to negate anticipation under 35 USC §102 (*Connell v. Sears, Roebuck & Co.*, 220 USPQ 193, 198 (Fed. Cir. 1983)). Thus, because Feldmeier '886 fails to disclose or teach "an array of binary CAM cells segmented into a plurality of array groups, each array group assigned a priority and each array group including a plurality of rows of CAM cells" and "a plurality of group global masks, each for storing a mask pattern indicating priority of a corresponding array group," as recited in Applicants' Claim 29, Feldmeier '886 neither anticipates nor renders obvious Claim 29. Accordingly, Applicants respectfully request the Examiner to withdraw the rejection of Claim 29 over Feldmeier '886.

Note that the amendments to Claim 29 incorporate language that appears in previously added Claim 73. Thus no new matter has been added, and Applicants' amendment does not necessitate a new search.

Claims 30, 32-38, and 59 depend from Claim 29, and therefore distinguish over the cited references for the same reasons as Claim 29.

Claims 73-74

Applicants' Claim 73 recites:

A content addressable memory (CAM) comprising:

a plurality of CAM array groups each including a plurality

of rows of binary CAM cells; and

means for assigning a first priority to a first and a second of the CAM array groups, and for assigning a second priority to a third of the CAM array groups, wherein the first and second priorities are different, and wherein the third CAM array group occupies an address space numerically between address spaces occupied by the first and second CAM array groups.

First, as discussed above with respect to Claim 29, Feldmeier '886 fails to disclose or suggest "a plurality of CAM array groups each including a plurality of rows of binary CAM cells," as recited in Applicants' Claim 73, nor has the Examiner pointed to any such language.

Second, while the CAM of Applicants' Claim 73 allows its array groups to be assigned priorities in any order, address entries in Feldmeier '886's CAM array must be stored (and maintained) in a predetermined order according to priority. Thus, in contrast to the Examiner's assertion, Feldmeier '886 teaches that the list of mask values are "sorted in hierarchical order" (col. 7, lines 39-40). Indeed, Feldmeier '886 specifically states that "the order of CAM entries is important. Address entries are stored in the CAM such that the addresses with masks with the largest number of trailing zeroes are stored first" (col. 8, lines 28-31). Accordingly, because Feldmeier '886 fails to disclose or suggest "means for assigning a first priority to a first and a second of the CAM array groups, and for assigning a second priority to a third of the CAM array groups, wherein the first and second priorities are different, and wherein the third CAM array group occupies an address space numerically between address spaces occupied by the first and second CAM array groups," as recited in Applicants' Claim 73, Claim 73 is patentable over Feldmeier '886.

Further, because Feldmeier '886 specifies that its binary address entries must be stored in a particular order according to priority, e.g., where "the addresses with masks with the largest number of trailing zeroes are stored first," Feldmeier '886 actually teaches away from Applicants' Claim 73. Accordingly, Applicants respectively request the Examiner to withdraw the rejection of Claim 73.

Claims 74-84 depend from Claim 73, and therefore distinguish over the cited references for at least the same reasons as Claim 73.

Rejection of Claims under 35 USC §102 over Ross

Claims 29-32, 36, and 73-74 are also rejected under 35 USC §102(e) as anticipated by U.S. Patent No. 6,389,506 to Ross. Applicants respectfully traverse these rejections, as discussed below.

Claims 29-32 and 36

Applicants' Claim 29 (as amended) recites:

A content addressable memory (CAM) system, comprising:

an array of binary CAM cells segmented into a plurality of array groups, each array group assigned a priority and each array group including a plurality of rows of CAM cells;

a plurality of group global masks, each for storing a mask pattern indicating priority of a corresponding array group; and

a priority table including a plurality of rows, each for storing the priority of a corresponding array group.

Ross neither discloses nor suggests the CAM system recited in Applicants' Claim 29.

The plurality of group global masks and the priority table are recited in Applicants' Claim 29 as separate circuit elements that may be used for separate and distinct functions. The

Examiner seems to equate Ross' block mask entry 220 with both the group global masks recited in Applicants' Claim 29 and the priority table recited in Applicants' Claim 29.

As mentioned above, to anticipate a claim under 35 USC §102, each and every element of the claim must be disclosed in a single reference, and the exclusion of a claimed element, no matter how insubstantial or obvious, from a prior art reference is enough to negate anticipation under 35 USC §102. Thus, assuming for arguments sake that Ross's block mask entry 220 discloses the group global masks that store mask patterns for corresponding array groups recited in Applicants' Claim 29, the Examiner has failed to point to any language in Ross that discloses or suggests a separate "priority table" that stores the priority of each array group, as recited in Applicants' Claim 29. Indeed, Ross is silent as to whether a separate table exists that stores priorities for corresponding array groups.

Thus, because Ross fails to disclose or teach each and every element recited in Applicants' Claim 29 (e.g., "a plurality of group global masks, each for storing a mask pattern indicating priority of a corresponding array group" and "a priority table including a plurality of rows, each for storing the priority of a corresponding array group" as recited in Applicants' Claim 29), Ross cannot properly form the basis of an anticipation rejection of Applicants' Claim 29 under 35 USC §102. Accordingly, Applicants respectfully request the Examiner to withdraw the rejection of Claim 29 over Ross.

Claims 30, 32-38, and 59 depend from Claim 29 and therefore distinguish over the cited references for at least the same reasons as Claim 29.

Claims 73-74

Applicants' Claim 73 recites:

A content addressable memory (CAM) comprising:

a plurality of CAM array groups each including a plurality of rows of binary CAM cells; and

means for assigning a first priority to a first and a second of the CAM array groups, and for assigning a second priority to a third of the CAM array groups, wherein the first and second priorities are different, and wherein the third CAM array group occupies an address space numerically between address spaces occupied by the first and second CAM array groups.

As discussed above with respect to Feldmeier '886, the CAM of Applicants' Claim 73 allows the array groups to be assigned priorities in any order (e.g., so that array groups having consecutively numbered groups of row addresses may store data in an out-of-order manner with respect to priority). There is no language in Ross that discloses or suggests that address entries can be stored in Ross' array in any order without regard to priority, nor has the Examiner pointed to any such language in Ross. As mentioned above, to anticipate a claim under 35 USC §102, each and every element of the claim must be disclosed in a single reference, and the exclusion of a claimed element, no matter how insubstantial or obvious, from a prior art reference is enough to negate anticipation under 35 USC §102. Accordingly, because Ross fails to disclose or suggest "means for assigning a first priority to a first and a second of the CAM array groups, and for assigning a second priority to a third of the CAM array groups, wherein the first and second priorities are different, and wherein the third CAM array group occupies an address space numerically between address spaces occupied by the first and second CAM array groups," Claim 73 is patentable over Ross.

Claims 74-84 depend from Claim 73, and therefore distinguish over the cited references for at least the same reasons as Claim 73.

Rejection of Claims under 35 USC §103

Claims 17-22, 59-62, 64-66, 69-70, 75-79, 89-93, and 99-100 are rejected under 35 USC §103(a) as being unpatentable over Feldmeier '886 or Ross in view of U. S. Patent No. 6,289,414 to Feldmeier (hereinafter referred to as Feldmeier '414). Applicants respectfully traverse these rejections, as discussed below.

Claims 17-20

Claims 17-20 now depend from Claim 16, which the Examiner has indicated as allowable over the cited references, and therefore Claims 17-20 distinguish over the cited references for at least the same reasons as Claim 16.

Claims 21-22

Claims 21 and 22 are canceled, and thus their rejections are now moot.

Claim 59

Claim 59 is amended to depend from Claim 29, which for reasons discussed above is patentable over the cited references. Therefore, Claim 59 distinguishes over the cited references for at least the same reasons as Claim 29.

Claims 60-62, 64-66, and 69-70

Applicants' Claim 60 recites:

A content addressable memory (CAM) comprising:

a plurality of CAM array groups each including a plurality of rows of binary CAM cells;

a plurality of group global mask circuits each coupled to a corresponding one of the CAM array group, wherein each group global mask circuit indicates a priority of the corresponding group of CAM cells relative to other CAM array groups; and

a plurality of mask valid bits, each indicating whether a valid global mask is stored in a corresponding group global mask circuit.

None of the cited references, whether taken alone or in combination, discloses or suggests the CAM recited in Applicants' Claim 60.

The Examiner acknowledges that neither Feldmeier '886 nor Ross "specifically discloses [a] plurality of mask valid bits, each indicating whether a valid global mask is stored in a corresponding group global mask circuit," and suggests that Feldmeier '414 discloses a "plurality of mask valid bits, each indicating whether a valid global mask is stored in a corresponding group global mask circuit (col. 2 lines 53-57) for the purpose of providing advantage of indicating the status of entry thereby preventing an error or saving access time by reading or writing only the status bits instead of entire line."

The Examiner then concludes that "it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate [a] plurality of mask valid bits, each indicating whether a valid global mask is stored in a corresponding group global mask circuit of 414 in the teaching of Feldmeier or Ross thereby [resulting] in an invention as claimed."

Applicants disagree. The language in Feldmeier '414 relied upon by the Examiner describes data valid bits that indicate whether rows of a CAM array store valid data. Specifically,

Feldmeier '414 states at col. 2 lines 53-57 that "data can be written directly into the first empty location [of the CAM array] because every location has a special status bit that keeps track of whether the location has valid information in it..." Later in the same paragraph, Feldmeier '414 notes that "CAMs also comprise a mask register which allows selection of which bits will participate in the comparison" (col. 2, lines 59-61). Notably, Feldmeier '414 fails to disclose or suggest a mask valid bit that indicates whether the mask register stores a valid mask. Thus, after reading the entire paragraph from which the Examiner extracts a few lines of text to support the rejection of Applicants' Claim 60, it is clear that the valid bits mentioned in Feldmeier '414 are for indicating the validity of data stored in rows of a CAM array; **NOT** for indicating the validity of a mask stored in a mask circuit.

Indeed, in contrast to the Examiner's suggestion, there is no language in Feldmeier '414 that discloses or suggests a mask valid bit that indicates whether a mask circuit stores a valid mask. Rather, the valid bits mentioned in the paragraph beginning at col. 2, line 47 in Feldmeier '414 and relied upon by the Examiner seem to correspond to the valid bits recited in Applicants' Claim 62, which recites "wherein each row of binary CAM cells further comprises a valid bit indicating whether valid data is stored in the row," which is consistent with the language provided by Feldmeier '414 in its. Accordingly, because Feldmeier '414 fails to disclose or suggest "a plurality of mask valid bits, each indicating whether a valid global mask is stored in a corresponding group global mask circuit," as recited in Applicants' Claim 60, Feldmeier '414 cannot properly form the basis of an obviousness rejection under 35 USC §103, as proposed by the Examiner. Therefore, Applicants' Claim 60 is patentable over the cited references.

Claims 61-62 and 64-72 depend from Claim 60 and therefore distinguish over the cited references for at least the same reasons as Claim 60.

Claims 75-79

Claims 75-79 depend from Claim 73, which for reasons discussed above Applicants believe to be patentable over the cited references, and therefore Claims 75-79 distinguish over the cited references for at least the same reasons as Claim 73.

Claims 89-93

Applicants' Claim 89 recites:

A content addressable memory (CAM) device, comprising:

a plurality of CAM array groups, each array group including a plurality of rows of CAM cells and a mask valid bit indicating whether the array group is assigned a priority relative to other array groups; and

an index circuit configured to generate a next free address (NFA) in response to the mask valid bits.

None of the cited references, whether taken alone or in combination, discloses or suggests the CAM device of Applicants' Claim 89.

The Examiner again notes that neither Feldmeier '886 nor Ross disclose "mask valid bits, each indicating whether a valid global mask is stored in a corresponding group global mask circuit," and again asserts that Feldmeier '414 discloses a "plurality of mask valid bits, each indicating whether a valid global mask is stored in a corresponding group global mask circuit..." As discussed above with respect to Claim 60, Feldmeier '414 fails to disclose or suggest a mask valid bit that indicates whether a corresponding mask circuit stores a valid mask. Therefore, in contrast to the Examiner's assertion,

Feldmeier '414 also fails to disclose or suggest "a mask valid bit indicating whether the array group is assigned a priority relative to other array groups," as recited in Applicants' Claim 89. Accordingly, Claim 89 is patentable over the cited references.

The Examiner also notes that neither Feldmeier '886 nor Ross disclose an "index circuit to generate a next free address (NFA) for the data according to its priority," and asserts that Feldmeier '414 discloses "an index circuit to generate a next free address (NFA) for the data according to its priority...." The Examiner then concludes that "it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate an index circuit to generate a next free address (NFA) for the data according to its priority of 414 in the teaching of Feldmeier ['886] or Ross..."

Applicants disagree. First, as discussed above, Feldmeier '414 fails to disclose or suggest "a mask valid bit indicating whether the array group is assigned a priority relative to other array groups," as recited in Applicants' Claim 89. Second, because Feldmeier '414 fails to disclose or suggest the "mask valid bits" recited in Applicants' Claim 89, Feldmeier '414 necessarily fails to disclose or suggest a circuit that generates a next free address (NFA) in response to the mask valid bits. Indeed, the Examiner has not pointed to any language in the cited references that discloses or suggests "an index circuit configured to generate a next free address (NFA) in response to the mask valid bits (emphasis added)," as recited in Applicants' Claim 89. Accordingly, the Examiner has not made a prima facie case of obviousness of Claim 89 under 35 USC §103. Therefore, Applicants respectively request the Examiner to withdraw the rejection of Claim 89.

Claims 90-98 depend from Claim 89, and therefore distinguish over the cited references for at least the same reasons as Claim 89.

Claims 99-100

Applicants' Claim 99 recites:

A method for providing a next free address (NFA) for a content addressable memory (CAM) having a number of array groups, each array group including a plurality of rows of CAM cells, comprising:

providing a number of mask valid bits, each indicating whether a corresponding array group is assigned a priority; and

generating the NFA in response to the mask valid bits.

None of the cited references, whether taken alone or in combination, discloses or suggests the method of Applicants' Claim 99.

As discussed above with respect to Claims 60 and 89, none of the cited references, including Feldmeier '414, disclose or even suggest a mask valid bit indicating whether a corresponding array group is assigned a priority, and therefore none of the cited references, including Feldmeier '414, disclose or suggest an index circuit that generates a next free address in response to the mask valid bits. Accordingly, in contrast to the Examiner's conclusion that "it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate generating a next free address (NFA) of 414 in the teaching of Feldmeier [886] or Ross," none of the cited references disclose or suggest "providing a number of mask valid bits, each indicating whether a corresponding array group is assigned a priority." Further, none of the cited references disclose or suggest "generating the NFA in response to the mask valid bits," as recited in Applicants' Claim 99. Accordingly,

the Examiner has failed to make a prima facie case of obviousness under 35 USC §103 of Applicants' Claim 99, and therefore Claim 99 is patentable over the cited references.

Claim 100 depends from Claim 99, and therefore distinguishes over the cited references for at least the same reasons as Claim 99.

Amendment of Claims 8, 10, 46-47, 59-60, and 69

Claims 8, 10, 46-47, 59-60, and 69 are voluntarily amended to correct clerical errors. These amendments are not narrowing and are not made for the purpose of patentability or avoiding the prior art.

CONCLUSION

In light of the above amendments and remarks, it is believed that Claims 1-20, 23-30, 32-40, 42-62, 64-84, and 89-100 are in condition for allowance and, therefore, a Notice of Allowance of Claims 1-20, 23-30, 32-40, 42-62, 64-84, and 89-100 is respectfully requested. If the Examiner's next action is other than allowance as requested, the Examiner is requested to call the undersigned at (415) 291-9497.

Respectfully submitted,

Dated: December 7, 2004

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CERTIFICATE OF MAILING
I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313-1450 on December 7, 2004.

By: _____
William L Paradice III